

STATUS OF THE CLAIMS

The status of the claims of the current application stands as follows:

Claims 1-6: (Cancelled)

7. **(Currently Amended)** An integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system, the architecture comprising:
 - a BIST for identifying and transmitting row and column addresses from failed embedded memory;
 - a first memory element for storing row addresses that have been assigned for repair by row redundancy;
 - a second memory element for storing column addresses that have been assigned for repair by column redundancy;
 - a third memory element for accumulating the failed row and column addresses transmitted from said BIST and assigning them each of the failed row and column addresses a particular weight value based on the number of like the failed row and column addresses already accumulated in said third memory element and their the relative locations of said failed row and column addresses within the memory system; and
 - means for allocating redundancy resources of the memory system assigning ones of the failed row and column addresses having weights greater than a threshold for permanent storage in said first or second memory element.
8. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said first, second, and third memory elements include the function of content addressable memory.
9. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said first memory element includes a register for storing row addresses that have been assigned for repair by row redundancy.
10. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said second memory element includes a register for storing column addresses

that have been assigned for repair by column redundancy.

11. **(Previously Presented)** An integrated redundancy architecture according to claim 7, wherein said third memory element includes a register for accumulating the failed row and column addresses transmitted from said BIST.
12. **(Previously Presented)** An integrated redundancy architecture according to claim 7, further comprising a finite state machine having a decision algorithm, said finite state machine in electrical communication with said first memory element, said second memory element, and said third memory element.
13. **(Previously Presented)** An integrated redundancy architecture according to claim 12, wherein said finite state machine allocates redundancy resources of said memory system according to said decision algorithm.
14. **(Previously Presented)** A method of providing BIST redundancy allocation to an embedded memory system, comprising the steps of:
 - a. identifying failed row and column addresses of defective memory blocks in said embedded memory system;
 - b. accumulating said failed row and column addresses identified in step a in a third memory element;
 - c. assigning failed row and column addresses accumulated in step b a particular weight value based on the number of like addresses already accumulated and their relative locations within the memory system; and
 - d. transferring said failed row and column addresses associated with the most fails from said third memory element to first and second memory elements according to a decision algorithm.
15. **(Previously Presented)** A method according to claim 14, wherein at least one of said first, second, and third memory elements include content addressable memory.
16. **(Previously Presented)** A method according to claim 14, wherein said first memory element includes a register for storing said failed row addresses.

17. **(Previously Presented)** A method according to claim 14, wherein said second memory element includes a register for storing said failed column addresses.
18. **(Previously Presented)** A method according to claim 14, wherein said third memory element includes a register for accumulating said failed row and column addresses transmitted from the BIST.
19. **(Previously Presented)** A method according to claim 14, wherein said steps c and d include using a finite state machine having a decision algorithm, said finite state machine being in electrical communication with said first memory element, said second memory element, and said third memory element.
20. **(Previously Presented)** A method according to claim 19, wherein said finite state machine allocates redundancy resources of said memory system according to said decision algorithm.
21. **(Previously Presented)** An integrated circuit comprising:
 - an embedded memory system having a plurality of row and column redundancies;
 - a BIST for identifying row and column addresses of defective memory blocks in said embedded memory system;
 - a first memory element;
 - a second memory element; and
 - a third memory element for accumulating said row and column addresses identified by said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations within the memory system.
22. **(Previously Presented)** An integrated circuit according to claim 21, further comprising a finite state machine having a decision algorithm, said finite state machine in electrical communication with said first memory element, said second memory element, and said third memory element.
23. **(Previously Presented)** An integrated circuit according to claim 22, wherein said finite state machine allocates redundancy resources of said memory system according to said

decision algorithm.

24. **(Previously Presented)** An integrated circuit according to claim 21, wherein at least one of said first, second, and third memory elements include content addressable memory.
25. **(Previously Presented)** An integrated circuit according to claim 21, wherein said first memory element includes a register for storing said failed row addresses.
26. **(Previously Presented)** An integrated circuit according to claim 21, wherein said second memory element includes a register for storing said failed column addresses.

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